



SEGA OF AMERICA, INC.
Consumer Products Division

IC BD 4M 32 PIN * 8 EPROM 32X R/D
837-11069
User's Manual

Doc. # MATI-47-08 1994

© 1994 SEGA. All Rights Reserved

1.0 Overview

This is one of the cards used in developing software for the Mega Drive / 32X.
Below is a list of its main features:

1. Can mount EPROM of up to 32 Mbit (4 Mbytes) on the card.
The EPROM used by this card uses a Toshiba TC594000AD series or equivalent product. Access time uses a device of 150 ns or less. This EPROM is not included.
2. An SRAM with a maximum 256 Kbit and battery backup function is installed.
3. Using the bank select function, any EPROM can be selected and accessed in 4-Mbit units. Bank numbers are valid from 0H to 7H.
4. Power Supply DC -5V is supplied from the main unit.
5. Has a memory mode switch function.
Can handle the conventional Mega Drive 16-Mbit mode via switch. Mode at factory shipment is the 32-Mbit mode.

2.0 Main Specifications

Product Number	837-11069
Print Circuit Board Number	171-6866
Memory Capacity	SRAM 32 Mbit (program area) SRAM 1 Mbit (data area)
Word Length	1 word 16 bits
Memory Expandability	Format Bank Selector
I/O Specifications	Conforms to Mega Drive cartridge connector specifications.
Card Dimensions	95.5 (W) 150 (H) mm
Pin Used:	General logic pins: TTL, LSI, IC EPROM: TC594006AD-150 (Toshiba) equivalent product SRAM: HM6286ALP1-12 (Hitachi) equivalent product Custom IC: 212-5719 (Sega) Battery: CR2032 (3mm) equivalent product Other: Electrolytic capacitor, chip capacitor, battery socket, DIP switch, etc.
Power supply	+5V
Temperature Range	0° C ~ 40° C
Relative Humidity	90% RH or less



3.0 Description of Functions

The SRAM card is managed by partitioning the memory address in 4 Mbits (bank 0 ~ bank 7, 32 Mbits). The Mega Drive cartridge area is partitioned into eight areas, each having 4 Mbits. Only area 0 with vector is fixed, and to the remaining seven areas, any bank can be allocated. Banks are specified by the bank setting register (Mega Drive A130F1F1 ~ A130F1FF odd addresses).

Bit 0 of register 0 is the address following 200000H used in switching the ROM side / backup RAM side. Bit 1 of register 0 is used in setting the backup RAM write protect. Because there is no bank for the backup RAM, addresses after 200000H become directly backup RAM area.

Bank numbers written in register 1 through register 7 correspond to their respective areas 1 through 7. Bank numbers can be set from 0 to 63; however with the RAM card, only the RAM installed bank numbers are effective. When 32 Mbits are loaded, only bank numbers from 0 to 7 are effective. The area will not function properly for any other setting.

When the power is turned on or reset, the cartridge area becomes 32 Mbit ROM mode (area 1 ~ area 7 : bank 1 ~ bank 7) space and write protect for the backup RAM is turned off. In this way, allocating all 32 Mbit address space to the MD cartridge area is called the ROM mode.

The next page shows the relationship between the MD cartridge area and bank setting register.

D7 D6 D5 D4 D3/D2 D1 D0

000000H Area 0
(permanent)

040000H Area 1

080000H Area 2

0C0000H Area 3

100000H Area 4

140000H Area 5

180000H Area 6

1C0000H Area 7

FCM area
or
Backup RAMRegister 0
(A130F14)

<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------

Register 1
(A130F34)

<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------

Register 2
(A130F54)

<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------

Register 3
(A130F74)

<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------

Register 4
(A130F94)

<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------

Register 5
(A130FB4)

<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------

Register 6
(A130FD4)

<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------

Register 7
(A130FF4)

<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------	--------------------------



ROM at 0, RAM at 1



Write to 0, not write to 1

BND - BND are bank numbers



Condition when the power is turned on or reset.

ROM Bank	MD Cartridge Area
Bank 0	Area 0 000000H
Bank 1	Area 1 000000H
Bank 2	Area 2 100000H
Bank 3	Area 3 100000H
Bank 4	Area 4 000000H
Bank 5	Area 5 000000H
Bank 6	Area 6 000000H
Bank 7	Area 7 000000H

Reg. 0 0000
 Reg. 1 0000
 Reg. 2 0000
 Reg. 3 0000
 Reg. 4 0000
 Reg. 5 0000
 Reg. 6 0000
 Reg. 7 0000

3.1 Using the 16 Mbit ROM Mode + Backup RAM

The SRAM card accommodates bank switching at shipment; therefore, it is 32 Mbit ROM space when initialized. As a result, the SRAM card is not compatible with a cartridge with 16 Mbit or less + backup RAM. (Existing memory map)

Changing DIP switch settings allows the use of 16 Mbit ROM + backup RAM. Because changing the DIP switch settings automatically results in the 16 Mbit ROM + backup RAM when the power is turned on or reset, changing the bank setting register is not necessary.

This applies to 000000H ~ 1FFFFFH ROM area, backup RAM area from 200000H. This type of memory allocation is called the 16M mode. Improper operation occurs if a bank register is changed in this mode.

Rex Sabio
242



3.2 Setting Switches with the Card

DIP switches are designed on the card, and 32 Mbit and 16 Mbit memory modes can be selected by setting these switches.

32 Mode (Factory settings)

SW135					
ON		ON		ON	ON
	OFF		OFF		
1	2	3	4	5	6

16 Mode (User settings)

SW135					
	ON			ON	ON
OFF		OFF	OFF		
1	2	3	4	5	6

3.3 Switch Descriptions

Switches 1 to 3 are used in chip select signal switching per each device.

Switch 4 Not used. Normally turned OFF.

Switch 5 Bank Register operation allowed/not allowed
ON Bank Register operation allowed
OFF Bank Register operation not allowed

Switch 6 Option Signal connectivity switching with device consideration
ON -CART signal connected
OFF -CART signal not connected

4.6 EPROM Mounting

This EPROM card has IC socket installed for IC 1 through IC 8. Programmed EPROM is used by being inserted to IC socket. Because the EPROM used by EPROM card is 512 Kbytes, use a minimum of two per word. (EPROM is installed to IC1 and IC3)

IC1, IC3, IC5, IC7 correspond to lower bytes (odd address, D0 - D7)

IC2, IC4, IC6, IC8 correspond to upper bytes (even address, D8 - D15).

Correlation with ROM banks is shown below:

IC1 and IC2 mount corresponds to bank 0 and bank 1

Mounted IC3 and IC4 corresponds to bank 2 and bank 3

Mounted IC5 and IC6 corresponds to bank 4 and bank 5

Mounted IC7 and IC8 corresponds to bank 6 and bank 7

The diagram on next page shows the EPROM's installing location.

Note When installing the EPROM, do so after checking the programmed pin no. 1



5.0 View

(Front View)

171-6866

